CLAIMS

Please amend claims 1-3, 9, and 13 as set forth below:

1. (Currently Amended) A device for calculating feedback signaling message (FSM) bits, comprising:

a circuit configured to calculate feedback signaling message (FSM) bits by means of which the signals sent from two antennas of a base station are influenced with reference to their phase difference and/or their amplitudes with the aid of two estimated channel impulse responses, wherein the ~~device~~circuit is in hard-wired form,

~~and~~ wherein the ~~device~~circuit is configured to generate a first complex phasor from first components of the two channel impulse responses and a second complex phasor from second components of the two channel impulse responses, and further configured to produce a[[n]] first FSM bit by a rotation and projection of the first phasor and a comparison of the rotated and projected first phasor with a constant threshold value and configured to produce a second FSM bit by a rotation and projection of the second phasor and a comparison of the rotated and projected second phasor with the constant threshold value,

and wherein the first and the second components of the two channel impulse responses comprise different components.

2. (Currently Amended) The device as claimed in claim 1,

wherein the components of the two channel impulse responses are applied at inputs of the ~~device~~circuit, and wherein

control signals are applied at control inputs of the ~~device~~circuit, and wherein

the FSM bit is provided at an output of the ~~device~~circuit, the FSM bit being calculated as a function of the components of the two channel impulse responses and the control signals.

3. (Currently Amended) The device as claimed in claim 2,

wherein the ~~device~~circuit comprises a logic unit configure to receive and selectively arrange the two channel impulse responses, and a processing unit connected downstream of the logic unit configured to process the two channel impulse responses based on the selective arrangement thereof.

4. (Original) The device as claimed in claim 3,

wherein the components of the two channel impulse responses are present at inputs of the logic unit, wherein

the logic unit has outputs whose number is equal to the number of its inputs, and wherein

the inputs of the logic unit are connected to the outputs of the logic unit as a function of at least one of the control signals.

5. (Original) The device as claimed in claim 3,

wherein the processing unit comprises a multiplier stage, an adder, a weighting stage, an accumulator and a threshold value decision unit connected in series in the prescribed sequence.

6. (Original) The device as claimed in claim 5,

wherein the multiplier stage has two multipliers whose inputs are connected in each case to two outputs of the logic unit, and wherein

the inputs of the adder are connected to the outputs of the multipliers.

7. (Original) The device as claimed in claim 6,

further comprising a control signal coupled as an input to the weighting stage, and

wherein the weighting stage is configured to apply a weighting factor to a sum formed by the adder as a function of the control signal coupled thereto.

8. (Original) The device as claimed in claim 2,

wherein the control signals are stored in the form of control bits in a read-only memory.

9. (Currently Amended) The device as claimed in claim 1, wherein the ~~device~~circuit is designed for the UMTS standard.

10. (Original) The device as claimed in claim 9,

wherein the control signals are a function of the slot number of the FSM bit to be calculated, and of a CLTD mode.

11. (Original) The device as claimed in claim 10,

wherein the control signals are a function of whether the slot number of the FSM bit to be calculated is an even or odd number.

12. (Original) A mobile radio terminal having a device as claimed in claim 1.

13. (Currently Amended) A method for calculating FSM bits utilizing a device which determines antenna weightings of a base station ~~by means of which the signals sent from two antennas of a base station are influenced with reference to their phase difference and/or their amplitudes with the aid of two estimated channel impulse responses~~, comprising:

~~(a)~~ producing a first complex phasor from first components of ~~the~~ two estimated channel impulse responses and a second complex phasor from second components of the two estimated channel impulse responses; and

~~(b)~~ calculating a[[n]] first FSM bit by rotation and projection of the first phasor and a second FSM bit by rotation and projection of the second phasor,

wherein the first and second FSM bits influence signals sent from two antennas of a base station with reference to their phase difference and/or their amplitudes with

the aid of the two estimated channel impulse responses,

and wherein the first and the second components of the two channel impulse responses comprise different components.

14. (Original) The method as claimed in claim 13,

wherein the rotation and projection of the phasor is determined by control signals.

15. (Original) The method as claimed in claim 13,

wherein calculating the FSM bit comprises performing a threshold value comparison after the rotation and projection of the phasor.

16. (Original) The method as claimed in claim 14, wherein the method is designed for the UMTS standard.

17. (Original) The method as claimed in claim 16,

wherein the control signals are a function of the slot number of the FSM bit to be calculated, and of a CLTD mode.

18. (Original) The method as claimed in claim 17,
wherein the control signals are a function of whether the slot number of the FSM bit to be calculated is an even or odd number.